

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"4368514":pn	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L2	298	(first or second) adj1 (processor or cpu) with (shar\$3 near3 (RAM or memory))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L3	5	((first or second) adj1 (processor or cpu) with (shar\$3 near3 (RAM or memory))) with clock\$1	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L4	41	((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with synchronous\$4	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L5	2	(((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with (shar\$3 near3 (RAM or memory))) and (((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with synchronous\$4)	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L6	46	(clock near3 generat\$3) with (multiprocessor)	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L7	55	(clock near3 generat\$3) with (multiprocessor or multi-processor)	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L8	56	((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with phase	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L9	46	((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with (RAM or memory) with clock\$1	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L10	601	(memory adj1 array) with (memory adj1 controller)	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L11	138	((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with (shar\$3 near3 (RAM or memory))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L12	1	((memory adj1 array) with (memory adj1 controller)) same (multi-processor or (multi adj1 processor))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L13	0	((memory adj1 array) with (memory adj1 controller)) and (((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with (shar\$3 near3 (RAM or memory)))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52

L14	1234	(memory adj1 array) same (memory adj1 controller)	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L15	2	((memory adj1 array) same (memory adj1 controller)) and (((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with (shar\$3 near3 (RAM or memory)))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L16	686	(memory adj1 array) same (memory adj1 controller) same address\$2	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L17	14	((memory adj1 array) same (memory adj1 controller) same address\$2) and ((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L18	3	((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with (disabl\$3 near3 clock)	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L19	1	(disabl\$3 near3 clock) same (multi-processor or (multi adj1 processor))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L20	9	(disabl\$3 near3 clock) with ((first or second) adj1 (processor or cpu))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L21	14	((disabl\$3) with ((first or second) adj1 (processor or cpu))) with clock\$1	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L22	146	(disabl\$3) with ((first or second) adj1 (processor or cpu))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L23	2235	713/32\$.ccls.	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L24	55	713/32\$.ccls. and ((first adj1 (processor or cpu)) with (second adj1 (processor or cpu)))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L25	73	713/32\$.ccls. and ((first adj1 (processor or cpu)) same (second adj1 (processor or cpu)))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L26	28	(713/32\$.ccls. and ((first adj1 (processor or cpu)) same (second adj1 (processor or cpu)))) and (stop\$3 near2 clock\$1)	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L27	10280	multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L28	854	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and (control\$3 near2 clock\$1)	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52

L29	340	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and ((stop\$3 or disabl\$3 or inhibit\$3) near2 clock\$1)	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L30	225	((multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and (control\$3 near2 clock\$1)) and ((multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and ((stop\$3 or disabl\$3 or inhibit\$3) near2 clock\$1))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L31	107	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and ((stop\$3 or disabl\$3 or inhibit\$3) near2 (clock\$1 near2 (output\$1 or signal\$1)))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L32	24	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and ((stop\$3 or disabl\$3 or inhibit\$3) near2 (clock\$1 near2 (output\$1)))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L33	889	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and (generat\$3 near2 clock\$1)	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L34	126	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and (selective\$3 near2 disabl\$3)	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L35	147	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and (selective\$3 near2 (disabl\$3 or inhibit\$3 or stop\$3))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L36	46	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and ((selective\$3 near2 (disabl\$3 or inhibit\$3 or stop\$3)) with (processor\$1 or cpu\$1))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L37	29	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and ((selective\$3 near2 (disabl\$3 or inhibit\$3 or stop\$3)) with (clock\$1))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L38	24	suspend\$3 near3 (second adj1 processor)	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52

L39	3578	external near3 reset	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L40	891	external near3 reset adj1 signal\$1	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L41	1273	external near3 (reset adj1 signal\$1)	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L42	13	(external near3 (reset adj1 signal\$1)) and (multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L43	0	(external near3 (reset adj1 signal\$1)) and (multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1))	EPO; JPO; IBM_TDB	OR	OFF	2005/03/23 11:52
L44	194	external near3 (reset adj1 signal\$1)	EPO; JPO; IBM_TDB	OR	OFF	2005/03/23 11:52
L45	0	first adj1 (external near3 (reset adj1 signal\$1))	EPO; JPO; IBM_TDB	OR	OFF	2005/03/23 11:52
L46	18	first adj1 (external near3 (reset adj1 signal\$1))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L47	225	(high adj2 (processor or cpu)) with (low adj2 (processor or cpu))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L48	11	((high adj2 (processor or cpu)) with (low adj2 (processor or cpu))) and 713/32\$.ccls.	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L49	5	"6240521".URPN.	USPAT	OR	OFF	2005/03/23 11:52
L50	13	(first or second) adj1 external adj1 reset	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L51	2	"973888"	US-PGPUB	OR	OFF	2005/03/23 11:52
L52	1	"5903503".pn.	USPAT	OR	OFF	2005/03/23 11:52
L53	6	(phase near2 synchroni\$7) same (second adj1 (processor or CPU))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L54	15	"5631591".URPN.	USPAT	OR	OFF	2005/03/23 11:52
L55	0	(phase near2 align\$6) same (second adj1 (processor or CPU))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L56	81	(phase near2 synchroni\$7) same (memory with (processor or CPU))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L57	6	(phase\$1 near2 synchroni\$7) same (second adj1 (processor or CPU))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L58	0	(phase\$1 near2 align\$6) same (second adj1 (processor or CPU))	US-PGPUB; USPAT	OR	OFF	2005/03/23 11:52
L59	6	"5903747".URPN.	USPAT	OR	OFF	2005/03/23 11:52
L60	11	"5510740".URPN.	USPAT	OR	OFF	2005/03/23 11:52

L61	1	"6118314".URPN.	USPAT	OR	OFF	2005/03/23 11:52
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